



IVerifySpec™

Closed Loop Requirement Verification™

OVERVIEW

Design Verification is estimated to consume about 70% of resources for chip development. With the complexity of the designs rising, verification planning and management is critical to reducing the risk associated with complex product development. Developing a verification plan is one thing and keeping it in sync with the requirements as they evolve is quite another challenge. Manually keeping the requirements, the plan, the execution environment in sync compounds the problem. Analysis of execution results is daunting as a large amount of data is generated in the process. Globally distributed teams executing the plan add another dimension of the complexity. What is needed is a tool and methodology that automatically keeps all these facets in sync and is devoid of any manual error prone tasks.

THE IVerifySpec™ SOLUTION

IVerifySpec™ comprehensively manages verification of complex designs over a distributed environment. Engineers and verification architects create an executable verification plan that is dependent on the base design requirements. Key Verification Performance Indicators (VPI) are chosen for each of the requirements. This can include any metric considered important for the verification of the requirement such as code coverage, functional coverage, test results, assertions etc. As the requirements evolve the plan is automatically updated. The plan serves as a contract between the Design/Verification management and the verification team. It drives the verification execution process from which the VPI's are automatically extracted and captured in a database and annotated back onto the original plan for easy correlation. This requirement-driven verification brings quick and efficient closure to the verification process.

REQ:5 The rdy_acpt block implements a simple handshake protocol. When the device upstream from the interleaver drives data to it, the data is driven and the ready signal (di_rdy) is asserted. The upstream block asserts the data along with its rdy signal and must leave them asserted until the downstream block asserts its accept (di_acpt) signal.

name	Handshake block					
description	Handshaking between rdy_acpt block of upstream and downstream					
requirements	5					
features	description	link	type	curr.	prev.	bugs
Assertion	Handshaking between upstream block and downstream block	di_handshake	Assertion	Pass	Pass	
Assertion	Handshaking between upstream block and downstream block	do_handshake	Assertion	Pass	Pass	
Assertion		di_data_hold	Assertion	Pass	Pass	
Assertion		do_data_hold	Assertion	Pass	Pass	
Covergroup		sm_cvg	CoverGroup	70.00	70.00	89 76

FLOW BENEFITS

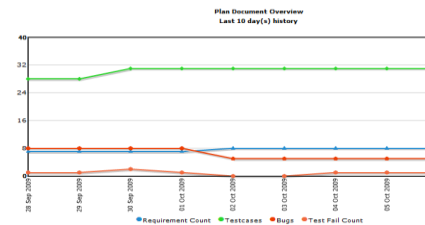
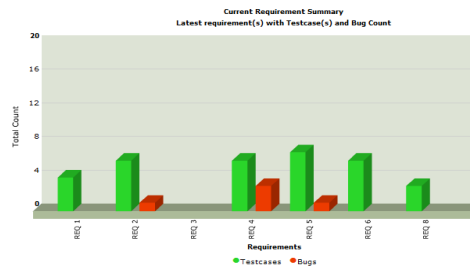
- ✓ Shortens verification time
- ✓ Keeps design/verification requirements, plan, execution and analysis in-sync.
- ✓ Allows teams to focus resources on critical areas in verification plan and execution
- ✓ Creates a systematic, automated, verification planning and execution environment
- ✓ Single environment for requirements, verification plan, metrics, bugs and schedule
- ✓ Provides key metrics for tape-out go/no-go decisions

COMPREHENSIVE VERIFICATION PLANNING & MANAGEMENT

FEATURES

- ❖ Automatic Links to requirement document thru LiveDocLink™ technology.
- ❖ Supports all major EDA vendors – Mentor Graphics, Synopsys, Cadence.
- ❖ Links to popular bug-tracking systems
- ❖ Imports/exports project plans to/from MS Project
- ❖ Web-based Verification Analysis Engine with real time data
- ❖ Historically track Verification Performance Indicator (VPI)
- ❖ Drill-down details for each VPI for debug and analysis
- ❖ Monitor progress against established verification Policy
- ❖ All verification technologies supported: simulation, formal, hardware emulation and assertion based verification.
- ❖ Various charts and analysis available
- ❖ User customizable reports and charts possible

Test2	Last 10 Day(s) History									
	Sep. 28	Sep. 29	Sep. 30	Sep. 01	Sep. 02	Sep. 03	Sep. 04	Sep. 05	Sep. 06	Sep. 07
add_cp										
di_data_hold										
di_hardware										
di_cvg										
di_delay										
diwave_data										
diwave_sync										
diwave_hold										
di_hardware										
in_hw										
in_hardware										
int_state										
out_hw										
out_hardware										
pk_start_check										



SPECIFICATION

Exports:

EDA tools: Mentor Graphics' Questa
Synopsys' VCS
Cadence's Incisive*

Project Management: MS Project, Jira*

Bug Tracking: Bugzilla, Jira*

Imports: Excel, CSV, TXT, MS Project

Industry Standards: DO-254

Packaging: Databases: MySQL, Oracle, PostgreSQL
Web servers : Apache Tomcat, RedHat JBoss.

Editors Supported: StarOffice, OpenOffice.org, MS Word*

OS Supported: Windows XP, Windows Vista, Linux, Solaris

* to be released

Agnisys, Inc. – Innovative Automation Delivered.

Agnisys is a pioneer in creating EDA products and services with extreme return on innovation. IDesignSpec (Register automation & management) and IVerifySpec (Verification planning & management) tools enable design and verification teams to exponentially improve productivity and QoR. 1255 Middlesex St. Unit 'I', Lowell, MA – 01851, USA. Email: info@agnisys.us Web: www.agnisys.us . Phone: 978-631-0505. Ver: IVS/2009/10/01/02

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