



IDesignSpec™

Register Automation and Management

OVERVIEW

As design size, complexity and time to market pressure grows, design teams focus on ways to improve productivity and quality. Lack of clarity in specification or errors in transcribing the specification into code can cause longer debug cycles or even stop-ships for products. The trend to use Intellectual Property (IP) makes it challenging to manage a large number of software addressable registers. IDesignSpec™ enables engineers to capture the hardware/software interface specification and automatically generate design code for all aspects of the design.

THE PROBLEM

Software addressable registers roughly amount to 20% of hardware design code. However, all teams working on the design are impacted by it. Hardware Design, Verification, Device Driver, Firmware, Lab Debug, Diagnostics, Software Development and Technical Publication teams depend on the an accurate, up-to-date description of these registers. Many of these teams require the register information coded in their own language, and following their own coding standard and format. Manually creating the register code for each of these groups is laborious, time consuming, error-prone and ultimately unproductive. The use of IP exacerbates the problem. Both internal, as well as external IP may not have all the views that each of the teams requires, this causes greater confusion and delays that can hamper the delivery of the SoC.

THE IDesignSpec™ SOLUTION

IDesignSpec™ comprehensively manages hardware/software interfaces for complex designs. Engineers create an executable specification for the memory map and all derived views are automatically generated from it. Complex, hierarchical, multi-dimensional registers can be described easily and intuitively. Consistency checks are performed up-front before any output is generated so that errors are eliminated at the source. The generated outputs can be easily customized using Tcl or XSLT or new outputs can be created without any compilation. IDesignSpec™ provides complete flexibility by providing interfaces to generated logic such that even complex and esoteric registers can be hand crafted and attached to the generated code. It is implemented as a plug-in for popular editors so that it is simple and easy to use and can be adopted without disruption to the current process.

FLOW BENEFITS

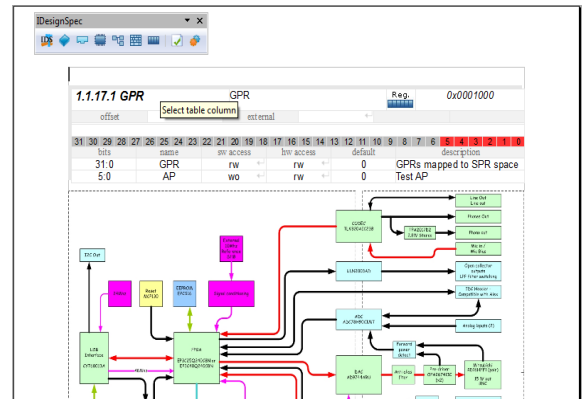
- ✓ Shortens development time and improves quality
- ✓ Plug-in to the corporate editor; no new tool needed.
- ✓ Eliminates bugs by creating correct-by-construction design files.
- ✓ Read in existing register definitions and standardize them across teams and products
- ✓ Easy and intuitive to use

REGISTER MAPS

FROM SPECIFICATION DOCUMENT
TO REAL CODE

FEATURES

- ❖ Describe registers inside functional specification documents.
- ❖ Self-checking “templates” prevent errors from entering the flow.
- ❖ Semantic errors are shown while editing the document.
- ❖ Hierarchical, multi-dimensional registers and memories are easily created.
- ❖ User defined or Automatic address calculation.
- ❖ Large number of inputs and outputs supported.
- ❖ Outputs are totally customizable using Tcl or XSLT.
- ❖ Hooks available for user-defined register RTL code.
- ❖ Specify special properties for various outputs
- ❖ Interactive or batch mode possible



SPECIFICATION

Generated Outputs:

RTL design: Synthesizable VHDL and Verilog.
AMBA-AHB, Avalon and proprietary busses are supported.

Verification: OVM Register 1.0 package for Mentor Graphics
VMM RALF 1.13 for Synopsys
IP-XACT 1.5 for Cadence.

Software: C/C++ header files with data structures.

Documentation: HTML, PDF, XML, Word

Industry Standards: IP-XACT - 1.4 & 1.5, SystemRDL 1.0

Imports: IP-XACT - 1.4 & 1.5, Excel, CSV, XML, Tcl, Txt

Packaging: IDesignSpec™ is available as an interactive editor based plug-in for MS Word, StartOffice, OpenOffice.org and Framemaker (beta). IDSBatch™ is a command line tool which enables further automation. Each of the output generators are available separately or bundled all together.

Editors Supported: MS Word, StarOffice, OpenOffice.org, Framemaker*

OS Supported: Windows XP, Windows Vista, Linux, Solaris

* to be released

Agnisys, Inc. – Innovative Automation Delivered.

Agnisys is a pioneer in creating EDA products and services with extreme return on innovation. IDesignSpec (Register automation & management) and IVerifySpec (Verification planning & management) tools enable design and verification teams to exponentially improve productivity and QoR. 1255 Middlesex St. Unit 'I', Lowell, MA – 01851, USA. Email: info@agnisys.us Web: www.agnisys.us . Phone: 978-631-0505. Ver: IDS/2009/10/01/02

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